WHAT IS CLAIMED IS:

1. A multi-layer circuit wiring board comprising a laminate of films, each film having a wiring pattern formed on at least one surface thereof, wherein the wiring pattern formed on each film is electrically connected with the wiring pattern formed on another film which is disposed neighboring thereto through a via-contact layer formed in any one of the neighboring films.

2. The multi-layer circuit wiring board according to claim 1, wherein all of said films have almost the same thickness.

3. A method of manufacturing a multi-layer circuit wiring board, which comprises: simultaneously laminating a second flexible resin film on one surface of a first flexible resin film having a first wiring pattern on at least one surface thereof, and a third wiring pattern on another surface of the first flexible resin film, said second flexible resin film having a second wiring pattern formed on at least one surface thereof, and said third flexible resin film having a third wiring pattern formed on at least one surface thereof.

4. A multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact

layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided on one surface thereof with a fourth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on the other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern; and

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern.

5. The multi-layer circuit wiring board according to claim 4, wherein said first film comprises a polyimide resin layer, and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; and said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer.

6. The multi-layer circuit wiring board according to claim 5, wherein a surface roughness of that surface of the polyimide resin layer on which said wiring pattern is formed, is within a range of 0.01μm to 5.0μm based on an average roughness as measured at optional ten points, said polyimide resin layer being at least one film selected from the group consisting of said first film, second film and third film.

7. The multi-layer circuit wiring board according to claim 5, wherein a line width of said wiring pattern formed on said polyimide resin layer is 50μm or less, said polyimide resin layer being at least one film selected from the group consisting of said first film, second film and third film, and a surface roughness of said polyimide resin layer is within a range of 0.01μm to 5.0μm based on an average roughness as measured at optional ten points.

8. The multi-layer circuit wiring board according to claim 5, which further comprises a first adhesive layer for bonding said second film to said first film, and a second adhesive layer for bonding said third film to said first film.

9. The multi-layer circuit wiring board according to claim 8, wherein said adhesive layers are formed of a thermosetting adhesive layer containing an epoxy curing component.

10. The multi-layer circuit wiring board according

to claim 8, wherein a thickness of each of said adhesive layers is 30μm or less.

11. The multi-layer circuit wiring board according to claim 4, wherein said first via-contact layer, second via-contact layer and third via-contact layer are formed of a blind via-contact layer, and a ratio of diameter of a bottom of each of these via-contact layers to diameter of a top opening of each of these via-contact layers is within a range of 0.2 to 1.0.

12. The multi-layer circuit wiring board according to claim 4, wherein said first via-contact layer, second via-contact layer and third via-contact layer are formed of a blind via-contact layer, and a ratio of diameter of a bottom of each of these via-contact layers to diameter of a top opening of each of these via-contact layers is within a range of 0.4 to 0.8.

13. The multi-layer circuit wiring board according to claim 4, wherein value of (value of a top opening of each of these via-contact layers)/(total value of a thickness of the conductor layer + a thickness of the second film or the third film + a thickness of the first adhesive layer or of the second adhesive layer) or value of (value of a top opening of each of these via-contact layers)/(total value of a thickness of the conductor layer + a thickness of the first film) is 1.5 or less.

14. A multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof; and

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

wherein said second film is provided with a first via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern.

15. The multi-layer circuit wiring board according to claim 14, wherein said first film comprises a polyimide resin layer and a first wiring pattern formed of copper and formed on said polyimide resin layer; and

said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on one surface of said polyimide resin layer.

16. The multi-layer circuit wiring board according to claim 14, which further comprises a fixing frame which is attached by means of an adhesive to that portion of an IC mounting surface on which said IC is not to be located.

17. The multi-layer circuit wiring board according to claim 16, which said fixing frame is made of a metal or resin.

18. A multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed

on another surface thereof, and a first via-contact layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided with a fourth wiring pattern on one surface thereof, another surface thereof being superimposed on the other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern;

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern;

a fourth film provided with a fifth wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said second film;

a fifth film provided on one surface thereof with a sixth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on said third film;

a fourth via-contact layer for electrically connecting said third wiring pattern with said fifth wiring pattern; and

a fifth via-contact layer for electrically connecting said fourth wiring pattern with said sixth

wiring pattern.

19. The multi-layer circuit wiring board according to claim 18, wherein said first film comprises a polyimide resin layer and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer; said fourth film comprises a polyimide resin layer and a fifth wiring pattern formed of copper and formed on said polyimide resin layer; and said fifth film comprises a polyimide resin layer and a sixth wiring pattern formed of copper and formed on said polyimide resin layer.

20. The multi-layer circuit wiring board according to claim 18, which further comprises:

a first adhesive layer for bonding said second film to said first film;

a second adhesive layer for bonding said third film to said first film;

a third adhesive layer for bonding said fourth film to said second film; and

a fourth adhesive layer for bonding said fifth film to said third film.

21. A multi-layer circuit wiring board comprising

a laminate of resin films, each resin film having a wiring pattern formed on at least one surface thereof, wherein the wiring pattern formed on one resin film is electrically connected with a wiring pattern formed on another resin film which is disposed next to said one resin film, through a via-contact layer provided on said one resin film or on said another resin film, a wiring pattern formed on an outermost resin film on one side of said laminate is a wiring pattern for mounting an IC, and a wiring pattern formed on another outermost resin film on another side of said laminate is a wiring pattern to be electrically connected with a printed wiring board.

22. An IC package comprising an IC, and a multi-layer circuit wiring board mounting said IC, wherein said multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided on one surface thereof with a fourth wiring pattern to be electrically connected

with a printed wiring board, another surface thereof being superimposed on said other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern; and

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern.

23. The IC package according to claim 22, wherein said first film comprises a polyimide resin layer and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; and said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer.

24. An IC package comprising an IC, a multi-layer circuit wiring board mounting said IC, and a printed wiring board mounting said multi-layer circuit wiring board, wherein said multi-layer circuit wiring board comprising:

a first film having a first wiring pattern formed on one surface thereof, a second wiring pattern formed on another surface thereof, and a first via-contact

layer electrically connecting said first wiring pattern with said second wiring pattern;

a second film provided with a third wiring pattern for mounting an IC on one surface thereof, another surface thereof being superimposed on said one surface of said first film;

a third film provided on one surface thereof with a fourth wiring pattern to be electrically connected with a printed wiring board, another surface thereof being superimposed on the other surface of said first film;

a second via-contact layer for electrically connecting said first wiring pattern with said third wiring pattern; and

a third via-contact layer for electrically connecting said second wiring pattern with said fourth wiring pattern.

25. The IC package according to claim 22, wherein said first film comprises a polyimide resin layer and a first and a second wiring patterns each formed of copper and formed on said polyimide resin layer; said second film comprises a polyimide resin layer and a third wiring pattern formed of copper and formed on said polyimide resin layer; and said third film comprises a polyimide resin layer and a fourth wiring pattern formed of copper and formed on said polyimide resin layer.

26. The IC package according to claim 22, which further comprises a first adhesive layer for bonding said second film to said first film, and a second adhesive layer for bonding said third film to said first film.

27. The IC package according to claim 26, wherein each of said adhesive layers is formed of a thermosetting adhesive layer containing an epoxy curing component.

28. The IC package according to claim 26, wherein the thickness of each of said adhesive layers is 30μm or less.

29. The IC package according to claim 22, wherein said first via-contact layer, said second via-contact layer and said third via-contact layer are all formed of a blind via-contact layer, and the ratio of the diameter of the bottom of each of these via-contact layer to the diameter of the top opening of each of these via-contact layer is within the range of 0.2 to 1.0.

30. The IC package according to claim 22, wherein said first via-contact layer, said second via-contact layer and said third via-contact layer are all formed of a blind via-contact layer, and the ratio of the diameter of the bottom of each of these via-contact layers to the diameter of the top opening of each of these via-contact layers is within the range of 0.4 to

0.8.

31. The IC package according to claim 22, wherein said IC is electrically connected with said multi-layer circuit wiring board by way of face-down bonding.

32. The IC package according to claim 22, wherein said IC is electrically connected with said multi-layer circuit wiring board by way of wire bonding using a gold or aluminum wire.

33. The IC package according to claim 22, wherein said IC is sealed with a resin.

34. The IC package according to claim 31, wherein said IC is laminated with a metal plate and then sealed.

35. A method of manufacturing a multi-layer circuit wiring board, said method comprising:

forming a first via-contact layer in a first film having a first conductor layer formed on one surface thereof, and a second conductor layer formed on another surface thereof, thereby electrically connecting said first conductor layer with said second conductor layer;

forming a first wiring pattern in said first conductor layer, and forming a second wiring pattern in said second conductor layer;

laminating a second film having a first insulating layer and a third conductor layer formed on said first insulating layer on said one surface of said first film in such a manner that said first insulating layer is in

contact with said one surface of said first film;

laminating a third film having a second insulating layer and a fourth conductor layer formed on said second insulating layer on the other surface of said first film in such a manner that said second insulating layer is in contact with said other surface of said first film;

forming a second via-contact layer electrically connecting said third conductor layer with said first wiring pattern, and forming a third via-contact layer electrically connecting said fourth conductor layer with said second wiring pattern;

forming a wiring pattern for mounting an IC on said first conductor layer; and

forming a wiring pattern to be electrically connected with a printed wiring board on said second conductor layer.

36. The method according to claim 35, wherein a roll-to-roll technique is employed for a formation of said first and second wiring patterns, for a formation of said first via-contact layer, for a lamination of said second film onto said first film, for a lamination of said third film onto said first film, for a formation of a wiring pattern for mounting said IC, for a formation of a wiring pattern to be electrically connected with said printed wiring board, for a formation of said second via-contact layer, and for a

formation of said third via-contact layer.

37. The method according to claim 35, wherein said first, second and third via-contact layers are respectively formed by a procedure where an ultraviolet laser having a wavelength of third harmonics or more is employed to form a via-hole, and scattered metal particles deposited at an edge of opening of said via-hole are removed by making use of at least one method selected from a physical polishing using said ultraviolet laser, a physical polishing using abrasive grains, and a chemical polishing by way of acid treatment, thereby obtaining said via-hole having an aspect ratio of 1.5 or less.

38. The method according to claim 35, wherein said first, second and third via-contact layers are respectively formed by a procedure where an ultraviolet laser having a wavelength of third harmonics or more is employed to form a via-hole, and scattered metal particles deposited at an edge of opening of said via-hole are removed by making use of a physical polishing using said ultraviolet laser, wherein at least one method selected from a physical polishing using abrasive grains, and a chemical polishing using acid treatment is employed before or after the first-mentioned physical polishing to polish said first, second, third and fourth conductor layers until the aspect ratio of said via-hole becomes 1.5 or less.

39. The method according to claim 35, wherein said first, second and third via-contact layers are respectively formed by a procedure wherein an ultraviolet laser having a wavelength of third harmonics or more is employed to form a via-hole, residues generated in the formation of said via-hole are removed by making use of a desmear treatment, the holes to be used for forming said via-contact layer is treated to provide the holes with conductivity, and said holes are subjected to an electrolytic plating to form said via-contact layer.

40. The method according to claim 35, wherein said first, second and third via-contact layers are respectively formed by a procedure wherein an ultraviolet laser having a wavelength of third harmonics or more is employed to form a blind via-hole, and residues generated in the formation of said via-hole are removed by making use of a desmear treatment using permanganate.

41. The method according to claim 40, wherein said desmear treatment is followed by a treatment to provide said via-hole with conductivity by means of a direct plating system using at least one material selected from the group consisting of a tin-palladium colloid-based catalyst, a conductive polymer and carbon graphite.

42. The method according to claim 40, wherein said

desmear treatment is followed by an electroless copper plating to provide said via-hole with conductivity.

43. The method according to claim 35, wherein said first, second and third via-contact layers are respectively formed by a procedure wherein an ultraviolet laser having a wavelength of third harmonics or more is employed to form a blind via-contact layer-forming hole, residues generated in the formation of said blind via-contact layer-forming hole are removed by making use of a desmear treatment using permanganate, said via-hole is treated using a tin-palladium-based catalyst to provide said via-hole with conductivity or said via-hole is subjected to electroless plating to provide said via-hole with conductivity, and said via-hole is subjected to electrolytic plating using two or more stages of electric density to thereby fill the interior of said blind via-contact layer-forming hole with a metal.

44. The method according to claim 35, wherein the formation of a wiring pattern in said first conductor layer, the formation of a wiring pattern in said second conductor layer, the formation of a wiring pattern in said third conductor layer and the formation of a wiring pattern in said fourth conductor layer are formed by a procedure wherein said first, second, third and fourth conductor layers are respectively chemically polished to confine the thickness thereof to fall

within the range of 3 to 12μm and to confine non-uniformity in thickness of each of these conductor layers to fall within 20% or less of the thicknesses of said first, second, third and fourth conductor layers, and redundant portions of said first, second, third and fourth conductor layers are selectively removed by means of etching treatment using a resist to thereby form predetermined wiring patterns in said first, second, third and fourth conductor layers.

45. The method according to claim 35, wherein the formation of a wiring pattern in said first conductor layer, the formation of a wiring pattern in said second conductor layer, the formation of a wiring pattern in said third conductor layer and the formation of a wiring pattern in said fourth conductor layer are formed by a procedure wherein said first, second, third and fourth conductor layers are respectively chemically polished to confine the thickness thereof to fall within the range of 0.5 to 3μm and to confine non-uniformity in thickness of each of these conductor layers to fall within 20% or less of the thicknesses of said first, second, third and fourth conductor layers, and said first, second, third and fourth conductor layers are respectively selectively subjected to plating using a resist to form a predetermined pattern, which is followed by chemical polishing of said first, second, third and fourth conductor layers to thereby

remove portions thereof other than the plated portions thereof, thereby forming predetermined wiring patterns in said first, second, third and fourth conductor layers.

46. The method according to claim 45, wherein said plating is performed by a process wherein said conductor layers are subjected to acid washing treatment after the formation of said resist, and then subjected to Cu-plating at a current density of 1 to $4A/dm^2$.

47. A method of manufacturing a multi-layer circuit wiring board, said method comprising:

forming a first via-contact layer in a first film having a first conductor layer formed on one surface thereof, and a second conductor layer formed on another surface thereof, thereby electrically connecting said first conductor layer with said second conductor layer;

forming a first wiring pattern in said first conductor layer, and forming a second wiring pattern in said second conductor layer;

laminating a second film having a first insulating layer and a third conductor layer formed on said first insulating layer on said one surface of said first film in such a manner that said first insulating layer is brought into contact with said one surface of said first film;

laminating a third film having a second insulating

layer and a fourth conductor layer formed on said second insulating layer on the other surface of said first film in such a manner that said second insulating layer is brought into contact with the other surface of said first film;

forming a second via-contact layer electrically connecting said third conductor layer with said first wiring pattern, and forming a third via-contact layer electrically connecting said fourth conductor layer with said second wiring pattern;

forming a predetermined wiring pattern respectively in said third conductor layer and in said fourth conductor layer;

laminating a fourth film over said wiring pattern of said third conductor layer, said fourth film having a third insulating layer and a fifth conductor layer formed on said third insulating layer;

laminating a fifth film over said wiring pattern of said fourth conductor layer, said fifth film having a fourth insulating layer and a sixth conductor layer formed on said fourth insulating layer;

forming a fourth via-contact layer electrically connecting the wiring pattern of said third conductor layer with said fifth conductor layer, and forming a fifth via-contact layer electrically connecting the wiring pattern of said fourth conductor layer with said sixth conductor layer;

forming a wiring pattern for mounting an IC on said fifth conductor layer; and

forming a wiring pattern to be electrically connected with a printed wiring board on said sixth conductor layer.

48. The method according to claim 47, wherein the formation of a wiring pattern in said first conductor layer, in said second conductor layer, in said third conductor layer, in said fourth conductor layer, in said fifth conductor layer and in said sixth conductor layer is performed by a procedure wherein with respect to a fine pattern-forming region of layer where a wire-working pitch of fine wiring pattern is finer than 30μm, these conductor layers are respectively chemically polished to confine the thickness thereof to fall within the range of 0.5 to 3μm and to confine non-uniformity in thickness of said fine pattern-forming region of layer to fall within 20% or less, and said fine pattern-forming region of layer is selectively subjected to plating using a resist to form a predetermined pattern, which is followed by chemical polishing thereof to thereby remove portions other than the plated portions thereof, thereby forming predetermined wiring patterns in said fine pattern-forming region of layer; and with respect to a residual region of layer other than said fine pattern-forming region of layer, these conductor layers are

respectively chemically polished to confine the thickness thereof to fall within the range of 3 to 12μm and to confine non-uniformity in thickness of said residual region of layer to fall within 20% or less, and said residual region of layer is selectively subjected to etching using a resist to remove redundant portions thereof, thereby forming predetermined wiring patterns in said residual region of layer.

49. A method of manufacturing a multi-layer circuit wiring board, said method comprising:

(a) forming a first via-contact layer in a first film having a first conductor layer formed on one surface thereof, and a second conductor layer formed on another surface thereof, thereby electrically connecting said first conductor layer with said second conductor layer;

(b) forming a first wiring pattern in said first conductor layer, and forming a second wiring pattern in said second conductor layer;

(c) laminating a second film having a first insulating layer and a third conductor layer formed on said first insulating layer on said one surface of said first film in such a manner that said first insulating layer is brought into contact with said one surface of said first film;

(d) laminating a third film having a second insulating layer and a fourth conductor layer formed on

said second insulating layer on the other surface of said first film in such a manner that said second insulating layer is brought into contact with the other surface of said first film;

(e) forming a second via-contact layer electrically connecting said third conductor layer with said first wiring pattern, and forming a third via-contact layer electrically connecting said fourth conductor layer with said second wiring pattern;

(f) forming a predetermined wiring pattern respectively in said third conductor layer and in said fourth conductor layer;

(g) laminating a fourth film over said wiring pattern of said third conductor layer, said fourth film having a third insulating layer and a fifth conductor layer formed on said third insulating layer;

(h) laminating a fifth film over said wiring pattern of said second conductor layer, said fifth film having a fourth insulating layer and a sixth conductor layer formed on said fourth insulating layer;

(i) forming a fourth via-contact layer electrically connecting the wiring pattern of said third conductor layer with said fifth conductor layer, and forming a fifth via-contact layer electrically connecting the wiring pattern of said fourth conductor layer with said sixth conductor layer;

repeating said steps (g) through (i) to thereby

form a required number of layers to form a laminate;

forming a wiring pattern for mounting an IC on an outermost conductor layer which is disposed on one surface of said laminate; and

forming a wiring pattern to be electrically connected with a printed wiring board on another outermost conductor layer which is disposed on the other surface of said laminate.

50. The method according to claim 49, wherein the formation of a wiring pattern in each of these conductor layers is performed by a procedure wherein with respect to a fine pattern-forming region of layer where a wire-working pitch of fine wiring pattern is finer than 30μm, these conductor layers are respectively chemically polished to confine the thickness thereof to fall within the range of 0.5 to 3μm and to confine non-uniformity in thickness of said fine pattern-forming region of layer to fall within 20% or less, and said fine pattern-forming region of layer is selectively subjected to plating using a resist to form a predetermined pattern, which is followed by chemical polishing thereof to thereby remove portions other than the plated portions thereof, thereby forming predetermined wiring patterns in said fine pattern-forming region of layer; and with respect to a residual region of layer other than said fine pattern-forming region of layer, these conductor layers are

respectively chemically polished to confine the thickness thereof to fall within the range of 3 to 12μm and to confine non-uniformity in thickness of said residual region of layer to fall within 20% or less, and said residual region of layer is selectively subjected to etching using a resist to remove redundant portions thereof, thereby forming predetermined wiring patterns in said residual region of layer.

51. A method of manufacturing a multi-layer circuit wiring board, said method comprising:

forming a first via-contact layer in a first film having a first conductor layer formed on one surface thereof, and a second conductor layer formed on another surface thereof, thereby electrically connecting said first conductor layer with said second conductor layer;

performing a patterning of said first conductor layer to form a first wiring pattern in said first conductor layer;

laminating a second film having a first insulating layer and a third insulating layer on said first wiring pattern in such a manner that said first insulating layer is brought into contact with said first wiring pattern;

forming a second via-contact layer in said second film, thereby electrically connecting said third conductor layer with said first wiring pattern;

performing a patterning of said third conductor

layer to form a second wiring pattern in said third conductor layer;

laminating a third film having a second insulating layer and a fourth insulating layer on said second wiring pattern in such a manner that said second insulating layer is brought into contact with said second wiring pattern;

forming a third via-contact layer in said third film, thereby electrically connecting said fourth conductor layer with said second wiring pattern;

performing a patterning of said fourth conductor layer to form a third wiring pattern in said fourth conductor layer; and

performing a patterning of said second conductor layer to form a fourth wiring pattern in said second conductor layer.